

# EVALUATION LABORATORY

Rating Report - Issue 1

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Provisional Data

## **Wespack** Phase Control Thyristor Types N1366JK080 to N1366JK140

Development Type No.: NX159JK080-140

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### Abstract

The N1366JK080-140 Wespack phase control thyristor range features a 38mm diameter silicon slice (manufacturing reference NLJ) mounted in a low profile, cold welded capsule.

Summary of changes to previous issue.	
Issue 1	First issue – Advance Data

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Provisional Data

## Wespack Phase Control Thyristor

### Types N1366JK080 to N1366JK140

Development Type No.: NX159JK080-140

#### Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
$V_{DRM}$	Repetitive peak off-state voltage, (note 1)	800-1400	V
$V_{DSM}$	Non-repetitive peak off-state voltage, (note 1)	800-1400	V
$V_{RRM}$	Repetitive peak reverse voltage, (note 1)	800-1400	V
$V_{RSM}$	Non-repetitive peak reverse voltage, (note 1)	900-1500	V

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
$I_{T(AV)M}$	Maximum average on-state current, $T_{sink}=55^{\circ}C$ , (note 2)	1366	A
$I_{T(AV)M}$	Maximum average on-state current, $T_{sink}=85^{\circ}C$ , (note 2)	924	A
$I_{T(AV)M}$	Maximum average on-state current, $T_{sink}=85^{\circ}C$ , (note 3)	481	A
$I_{T(RMS)M}$	Nominal RMS on-state current, $T_{sink}=25^{\circ}C$ , (note 2)	2718	A
$I_{T(d.c.)}$	D.C. on-state current, $T_{sink}=25^{\circ}C$ , (note 4)	2304	A
$I_{TSM}$	Peak non-repetitive surge $t_p=10ms$ , $V_{rm}=60\%V_{RRM}$ , (note 5)	15.9	kA
$I_{TSM2}$	Peak non-repetitive surge $t_p=10ms$ , $V_{rm}\leq 10V$ , (note 5)	17.5	kA
$I^2t$	$I^2t$ capacity for fusing $t_p=10ms$ , $V_{rm}=60\%V_{RRM}$ , (note 5)	$1.26 \times 10^6$	$A^2s$
$I^2t$	$I^2t$ capacity for fusing $t_p=10ms$ , $V_{rm}\leq 10V$ , (note 5)	$1.53 \times 10^6$	$A^2s$
$(di/dt)_{cr}$	Critical rate of rise of on-state current (note 6)	(continuous, 50Hz)	100
		(repetitive, 50Hz, 60s)	200
		(non-repetitive)	400
$V_{RGM}$	Peak reverse gate voltage	5	V
$P_{G(AV)}$	Mean forward gate power	4	W
$P_{GM}$	Peak forward gate power	30	W
$T_{j op}$	Operating temperature range	-40 to +125	$^{\circ}C$
$T_{stg}$	Storage temperature range	-40 to +150	$^{\circ}C$

#### Notes:-

- 1) De-rating factor of 0.13% per  $^{\circ}C$  is applicable for  $T_j$  below  $25^{\circ}C$ .
- 2) Double side cooled, single phase; 50Hz,  $180^{\circ}$  half-sinewave.
- 3) Cathode side cooled, single phase; 50Hz,  $180^{\circ}$  half-sinewave.
- 4) Double side cooled.
- 5) Half-sinewave,  $125^{\circ}C$   $T_j$  initial.
- 6)  $V_D=67\%V_{DRM}$ ,  $I_{TM}=2000A$ ,  $I_{FG}=2A$ ,  $t_r\leq 0.5\mu s$ ,  $T_{case}=125^{\circ}C$ .

**Characteristics**

	PARAMETER	MIN.	TYP.	MAX.	TEST CONDITIONS (Note 1)	UNITS
V <sub>TM</sub>	Maximum peak on-state voltage	-	-	1.45	I <sub>TM</sub> =1700A	V
V <sub>TM</sub>	Maximum peak on-state voltage	-	-	1.99	I <sub>TM</sub> =3700A	V
V <sub>T0</sub>	Threshold voltage	-	-	0.985		V
r <sub>T</sub>	Slope resistance	-	-	0.270		mΩ
(dv/dt) <sub>cr</sub>	Critical rate of rise of off-state voltage	1000	-	-	V <sub>D</sub> =80% V <sub>DRM</sub> , linear ramp, gate o/c	V/μs
I <sub>DRM</sub>	Peak off-state current	-	-	100	Rated V <sub>DRM</sub>	mA
I <sub>RRM</sub>	Peak reverse current	-	-	100	Rated V <sub>RRM</sub>	mA
V <sub>GT</sub>	Gate trigger voltage	-	-	3.0	T <sub>j</sub> =25°C V <sub>D</sub> =10V, I <sub>T</sub> =3A	V
I <sub>GT</sub>	Gate trigger current	-	-	300		mA
V <sub>GD</sub>	Gate non-trigger voltage	-	-	0.25	Rated V <sub>DRM</sub>	V
I <sub>H</sub>	Holding current	-	-	1000	T <sub>j</sub> =25°C	mA
t <sub>gd</sub>	Gate-controlled turn-on delay time	-	0.5	1.5	V <sub>D</sub> =67% V <sub>DRM</sub> , I <sub>T</sub> =1000A, di/dt=10A/μs,	μs
t <sub>gt</sub>	Turn-on time	-	1.0	2.0	I <sub>FG</sub> =2A, t <sub>r</sub> =0.5μs, T <sub>j</sub> =25°C	μs
Q <sub>rr</sub>	Recovered charge	-	1600	1750		μC
Q <sub>ra</sub>	Recovered charge, 50% Chord	-	900	-	I <sub>TM</sub> =1000A, t <sub>p</sub> =1000μs, di/dt=10A/μs,	μC
I <sub>rr</sub>	Reverse recovery current	-	100	-	V <sub>r</sub> =50V	A
t <sub>rr</sub>	Reverse recovery time, 50% Chord	-	18	-		μs
t <sub>q</sub>	Turn-off time	-	80	-	I <sub>TM</sub> =1000A, t <sub>p</sub> =1000μs, di/dt=10A/μs, V <sub>r</sub> =50V, V <sub>dr</sub> =80%V <sub>DRM</sub> , dV <sub>dr</sub> /dt=20V/μs	μs
		-	150	-	I <sub>TM</sub> =1000A, t <sub>p</sub> =1000μs, di/dt=10A/μs, V <sub>r</sub> =50V, V <sub>dr</sub> =80%V <sub>DRM</sub> , dV <sub>dr</sub> /dt=200V/μs	
R <sub>thJK</sub>	Thermal resistance, junction to heatsink	-	-	0.0270	Double side cooled	K/W
		-	-	0.0469	Anode side cooled	K/W
		-	-	0.0636	Cathode side cooled	K/W
F	Mounting force	10	-	20	Note 2.	kN
W <sub>t</sub>	Weight	-	135	-		g

Notes:-

- 1) Unless otherwise indicated T<sub>j</sub>=125°C.
- 2) For other clamp forces, please consult factory.

**Notes on Ratings and Characteristics**

1.0 Voltage Grade Table

Voltage Grade	$V_{DRM}$ $V_{DSM}$ $V_{RRM}$ V	$V_{RSM}$ V	$V_D/V_R$ DC V
08	800	900	560
10	1000	1100	700
12	1200	1300	810
14	1400	1500	930

2.0 Extension of Voltage Grades

This report is applicable to other voltage grades when supply has been agreed by Sales/Production.

3.0 De-rating Factor

A blocking voltage de-rating factor of 0.13%/°C is applicable to this device for  $T_j$  below 25°C.

4.0 Repetitive dv/dt

Standard dv/dt is 1000V/μs.

5.0 Snubber Components

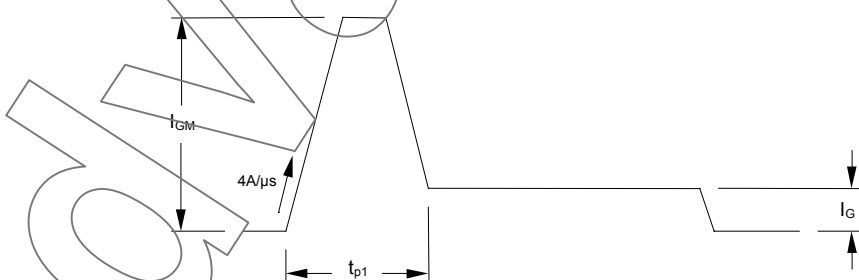
When selecting snubber components, care must be taken not to use excessively large values of snubber capacitor or excessively small values of snubber resistor. Such excessive component values may lead to device damage due to the large resultant values of snubber discharge current. If required, please consult the factory for assistance.

6.0 Rate of rise of on-state current

The maximum un-primed rate of rise of on-state current must not exceed 400A/μs at any time during turn-on on a non-repetitive basis. For repetitive performance, the on-state rate of rise of current must not exceed 200A/μs at any time during turn-on. Note that these values of rate of rise of current apply to the total device current including that from any local snubber network.

7.0 Gate Drive

The nominal requirement for a typical gate drive is illustrated below. An open circuit voltage of at least 30V is assumed. This gate drive must be applied when using the full di/dt capability of the device.



The magnitude of  $I_{GM}$  should be between five and ten times  $I_{GT}$ , which is shown on page 2. Its duration ( $t_{p1}$ ) should be 20μs or sufficient to allow the anode current to reach ten times  $I_L$ , whichever is greater. Otherwise, an increase in pulse current could be needed to supply the necessary charge to trigger. The 'back-porch' current  $I_G$  should remain flowing for the same duration as the anode current and have a magnitude in the order of 1.5 times  $I_{GT}$ .

8.0 Computer Modelling Parameters

8.1 Device Dissipation Calculations

$$I_{AV} = \frac{-V_{T0} + \sqrt{V_{T0}^2 + 4 \cdot ff^2 \cdot r_T \cdot W_{AV}}}{2 \cdot ff^2 \cdot r_T}$$

and:

$$W_{AV} = \frac{\Delta T}{R_{th}}$$

$$\Delta T = T_{j\max} - T_K$$

Where  $V_{T0}=0.985V$ ,  $r_T=0.270m\Omega$ ,

$R_{th}$  = Supplementary thermal impedance, see table below and

$ff$  = Form factor, see table below.

Supplementary Thermal Impedance							
Conduction Angle	30°	60°	90°	120°	180°	270°	d.c.
Square wave Double Side Cooled	0.0369	0.0348	0.0329	0.0314	0.0299	0.0277	0.0270
Square wave Cathode Side Cooled	0.0740	0.0716	0.0695	0.0677	0.0667	0.0641	0.0636
Sine wave Double Side Cooled	0.0350	0.0330	0.0315	0.0300	0.0278		
Sine wave Cathode Side Cooled	0.0719	0.0696	0.0679	0.0668	0.0643		

Form Factors							
Conduction Angle	30°	60°	90°	120°	180°	270°	d.c.
Square wave	3.46	2.45	2	1.73	1.41	1.15	1
Sine wave	3.98	2.78	2.22	1.88	1.57		

8.2 Calculating  $V_T$  using ABCD Coefficients

The on-state characteristic  $I_T$  vs.  $V_T$ , on page 6 is represented in two ways;

- (i) the well established  $V_{T0}$  and  $r_T$  tangent used for rating purposes and
- (ii) a set of constants A, B, C, D, forming the coefficients of the representative equation for  $V_T$  in terms of  $I_T$  given below:

$$V_T = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

The constants, derived by curve fitting software, are given below for both hot and cold characteristics. The resulting values for  $V_T$  agree with the true device characteristic over a current range, which is limited to that plotted.

25°C Coefficients		125°C Coefficients	
A	1.321808	A	4.19E-01
B	-8.55E-02	B	7.52E-02
C	1.19E-04	C	2.37E-04
D	1.28E-02	D	2.85E-04

8.3 D.C. Thermal Impedance Calculation

$$r_t = \sum_{p=1}^{p=n} r_p \cdot \left( 1 - e^{-\frac{t}{\tau_p}} \right)$$

Where  $p = 1$  to  $n$ ,  $n$  is the number of terms in the series and:

- $t$  = Duration of heating pulse in seconds.
- $r_t$  = Thermal resistance at time  $t$ .
- $r_p$  = Amplitude of  $p_{th}$  term.
- $\tau_p$  = Time Constant of  $r_{th}$  term.

The coefficients for this device are shown in the tables below:

D.C. Double Side Cooled				
Term	1	2	3	4
$r_p$	0.01628776	$5.61118 \times 10^{-3}$	$2.647435 \times 10^{-3}$	$2.309156 \times 10^{-3}$
$\tau_p$	0.2858404	0.09388713	0.02816524	$3.592634 \times 10^{-3}$

D.C. Cathode Side Cooled				
Term	1	2	3	4
$r_p$	0.04742413	0.01200315	$2.629734 \times 10^{-3}$	$1.66852 \times 10^{-3}$
$\tau_p$	1.793815	0.1311505	0.01493408	$2.829606 \times 10^{-3}$

9.0 Reverse recovery ratings

(i)  $Q_{ra}$  is based on 50%  $I_{rm}$  chord as shown in Fig. 1

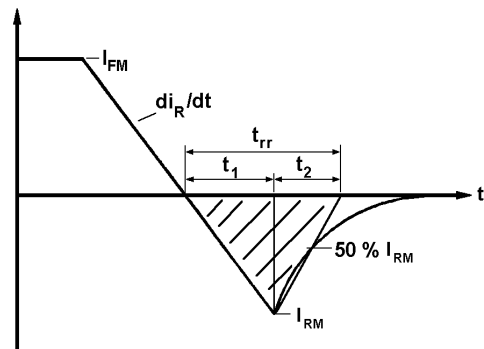


Fig. 1

(ii)  $Q_{rr}$  is based on a 150 $\mu$ s integration time i.e.

$$Q_{rr} = \int_0^{150 \mu s} i_{rr} \cdot dt$$

(iii)  $K \text{ Factor} = \frac{t_1}{t_2}$

**Curves**

Figure 1 – On-state characteristics of Limit device

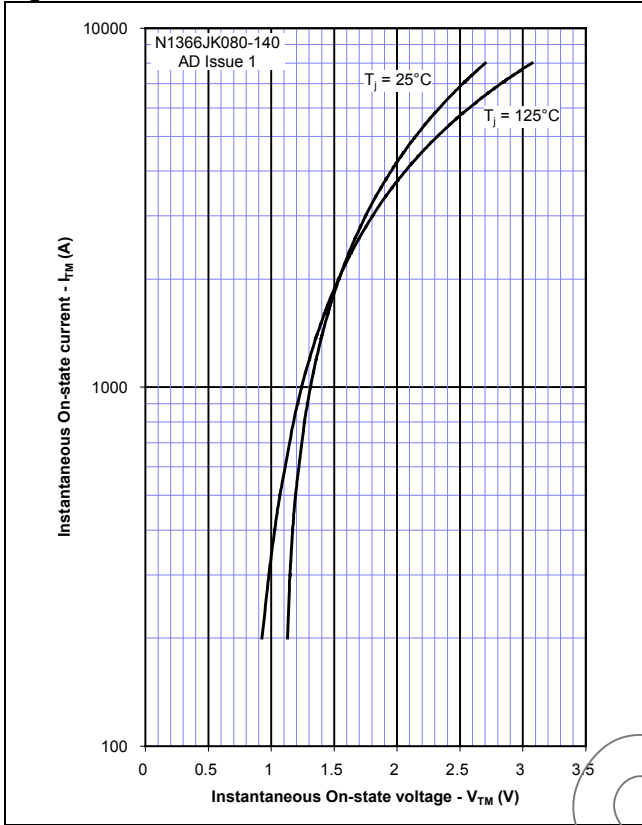


Figure 2 – Transient thermal impedance

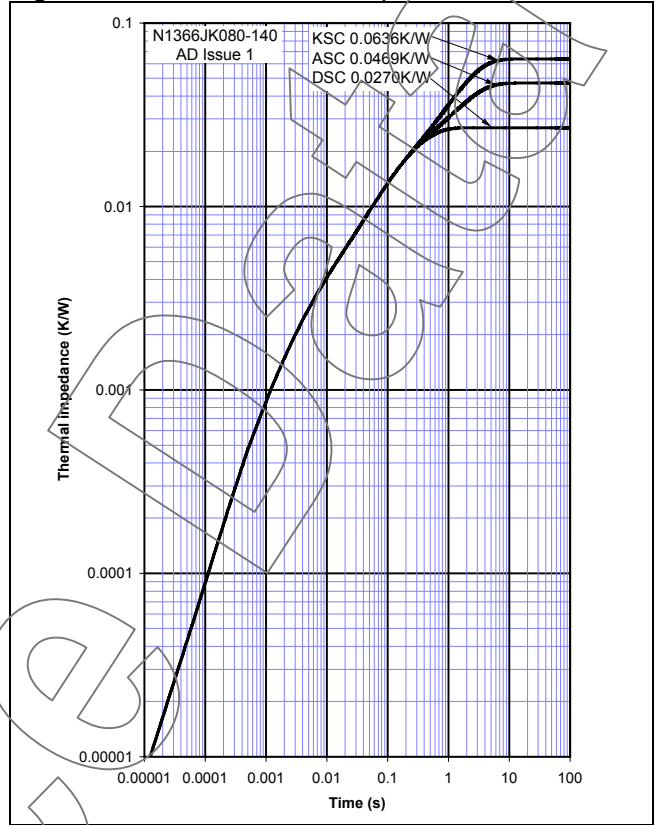


Figure 3 – Gate Characteristics – Trigger limits

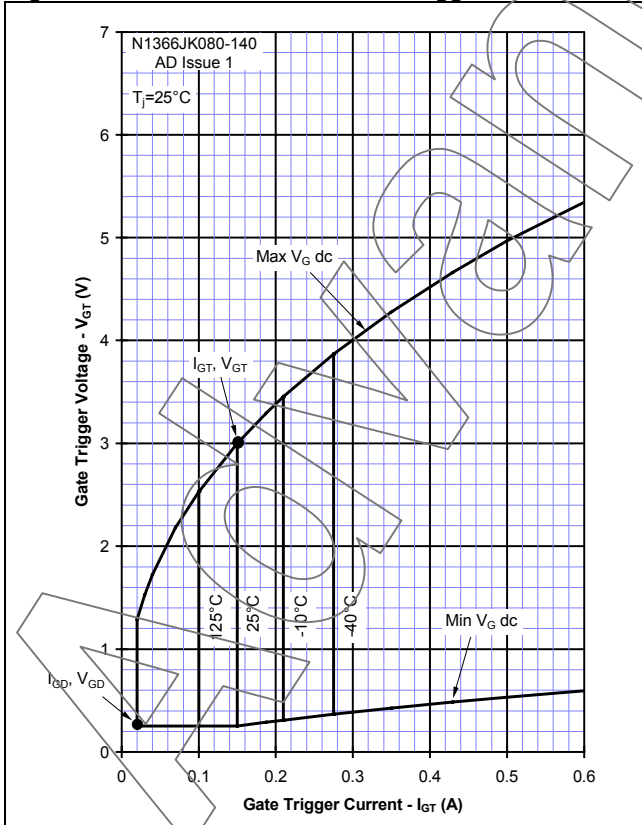


Figure 4 – Gate Characteristics – Power Curves

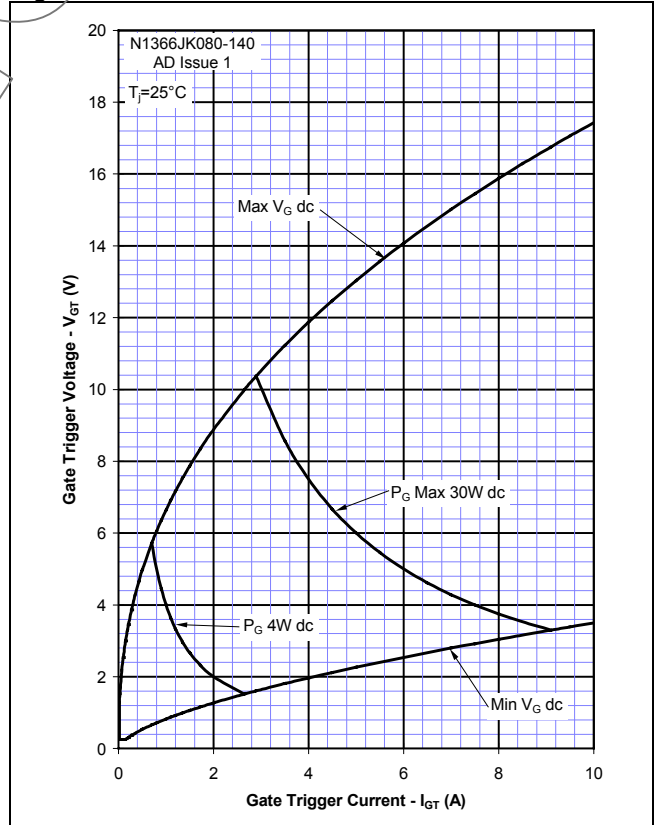




Figure 5 – Total Recovered Charge,  $Q_{rr}$

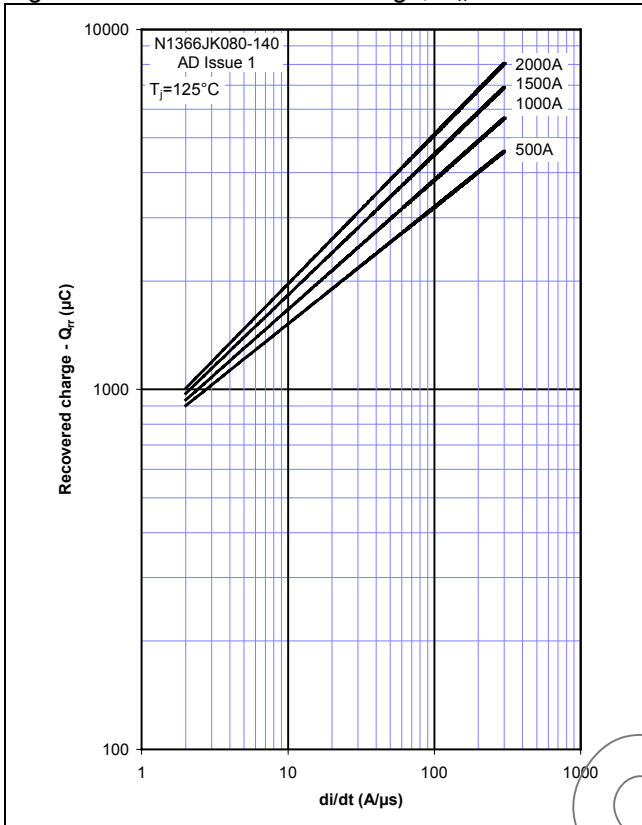


Figure 6 – Recovered Charge,  $Q_{ra}$  (50% chord)

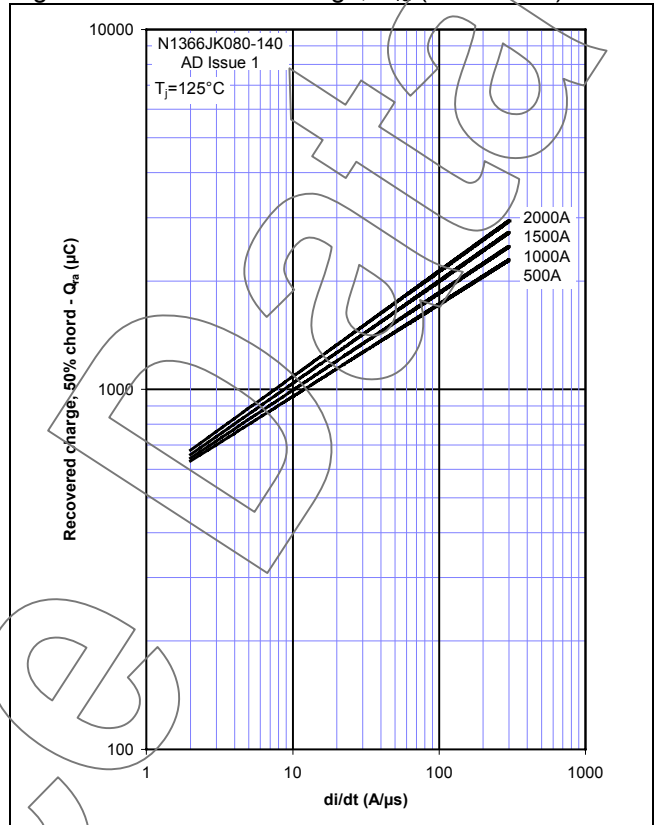


Figure 7 – Peak Reverse Recovery Current,  $I_{rm}$

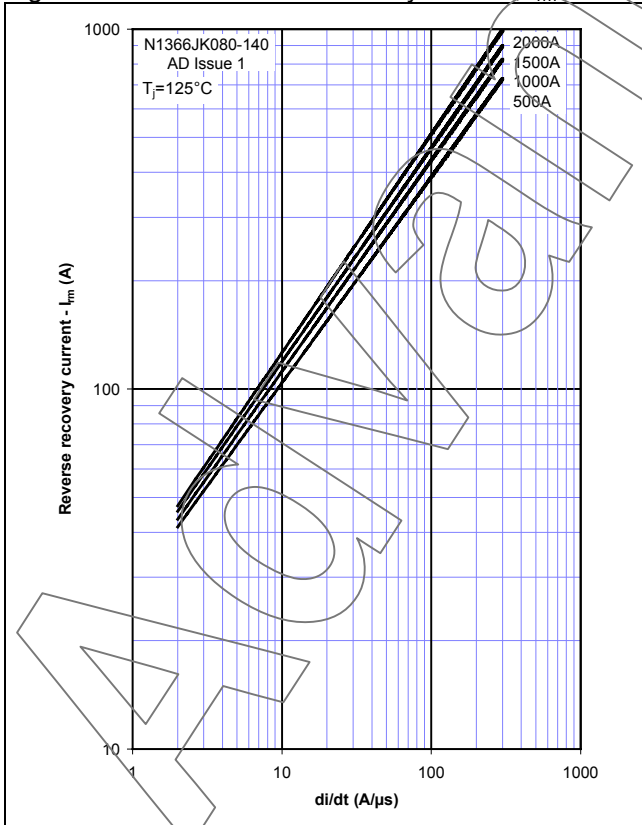


Figure 8 – Maximum Recovery Time,  $t_{rr}$  (50% chord)

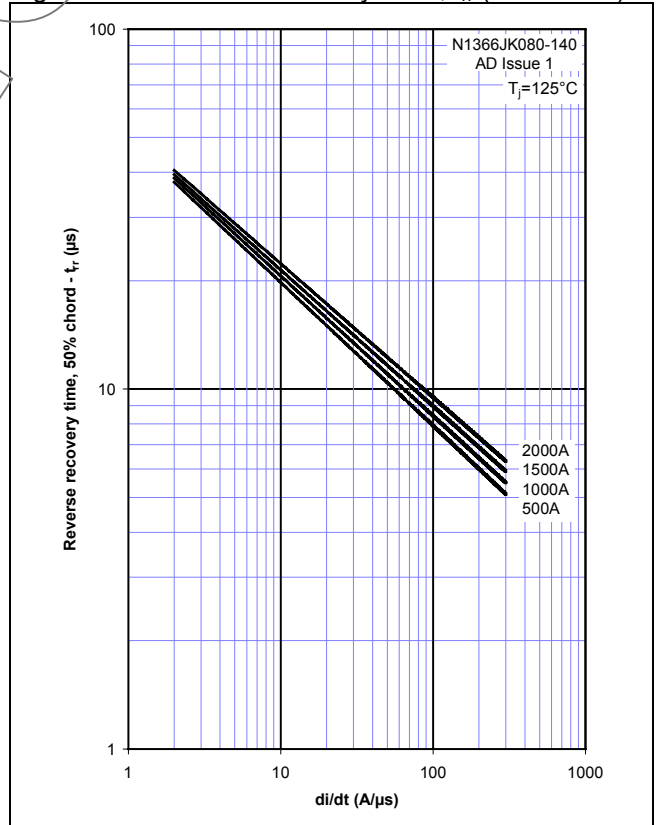


Figure 9 – On-state current vs. Power dissipation – Double Side Cooled (Sine wave)

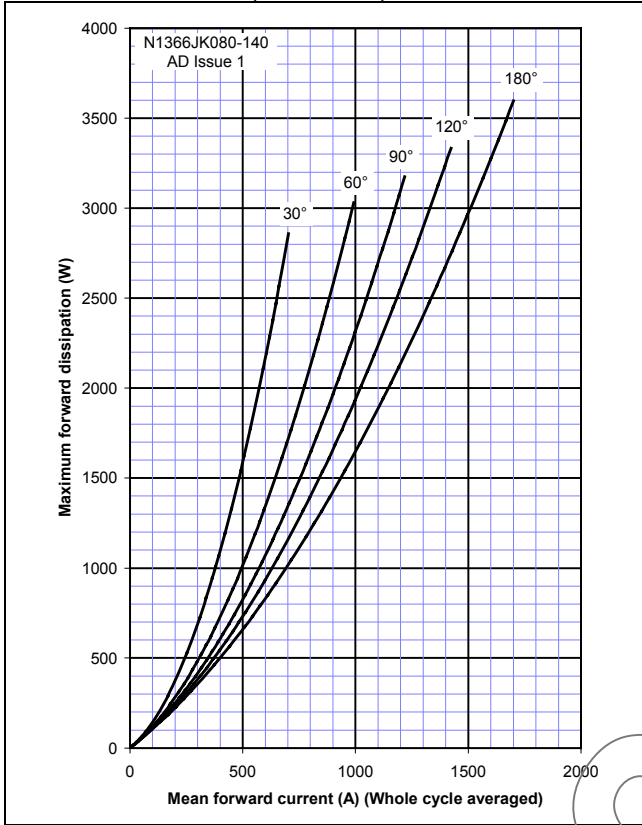


Figure 10 – On-state current vs. Heatsink temperature – Double Side Cooled (Sine wave)

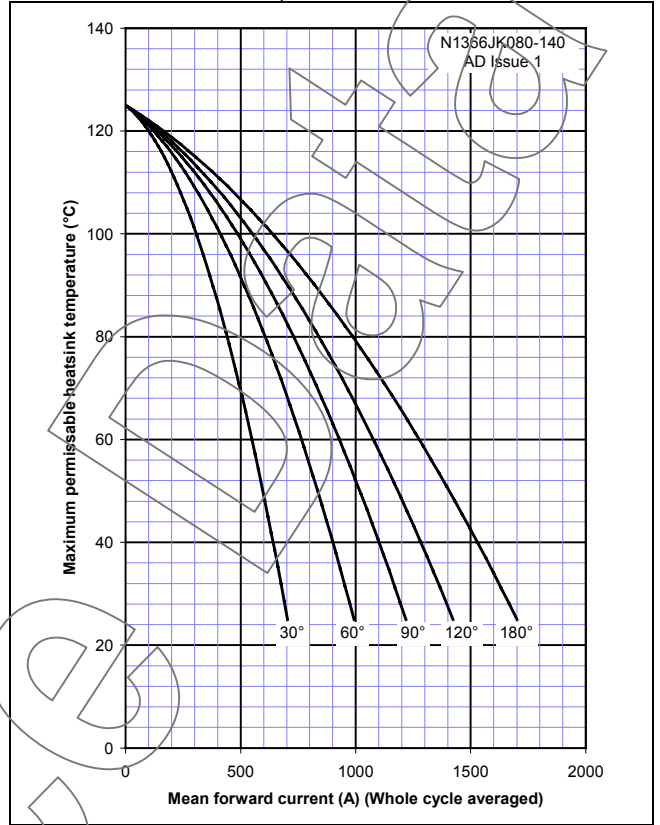


Figure 11 – On-state current vs. Power dissipation – Double Side Cooled (Square wave)

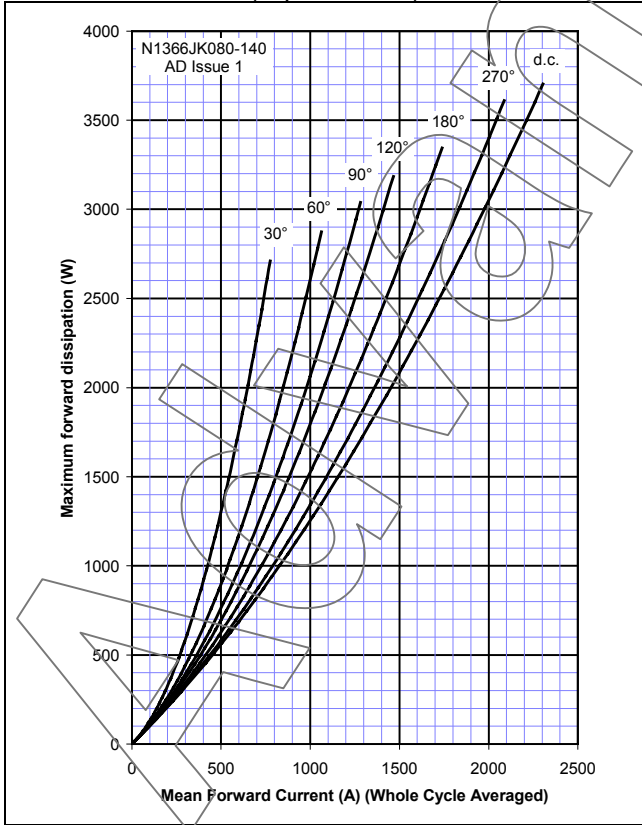


Figure 12 – On-state current vs. Heatsink temperature – Double Side Cooled (Square wave)

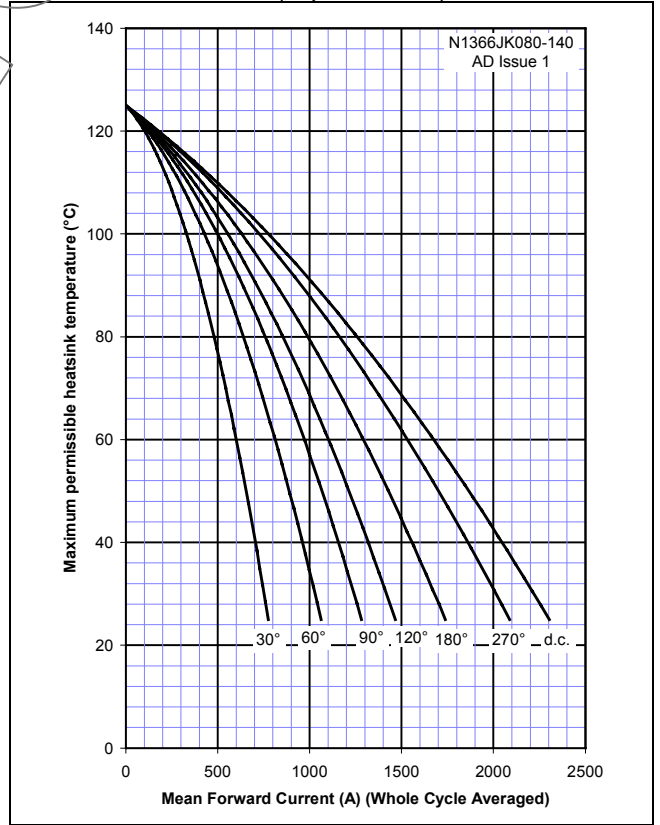


Figure 13 – On-state current vs. Power dissipation – Cathode Side Cooled (Sine wave)

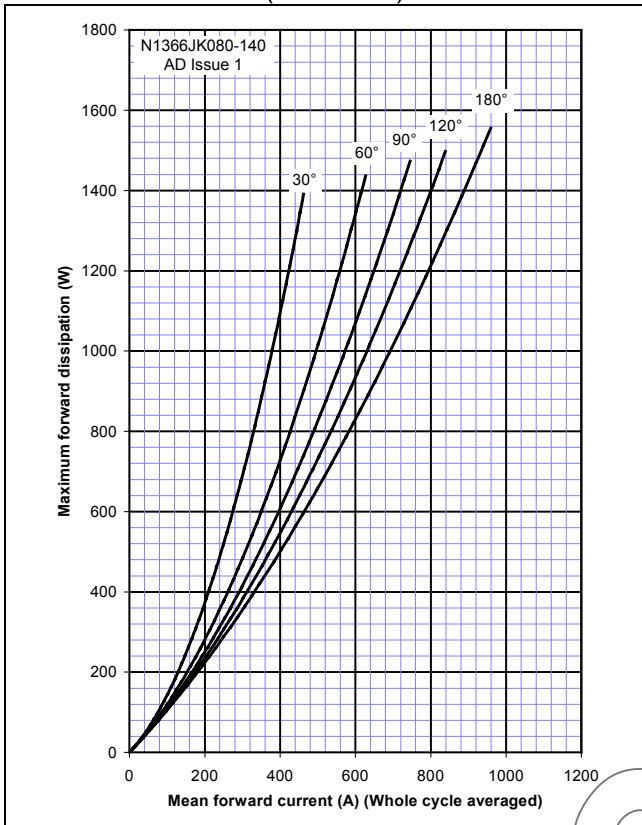


Figure 14 – On-state current vs. Heatsink temperature – Cathode Side Cooled (Sine wave)

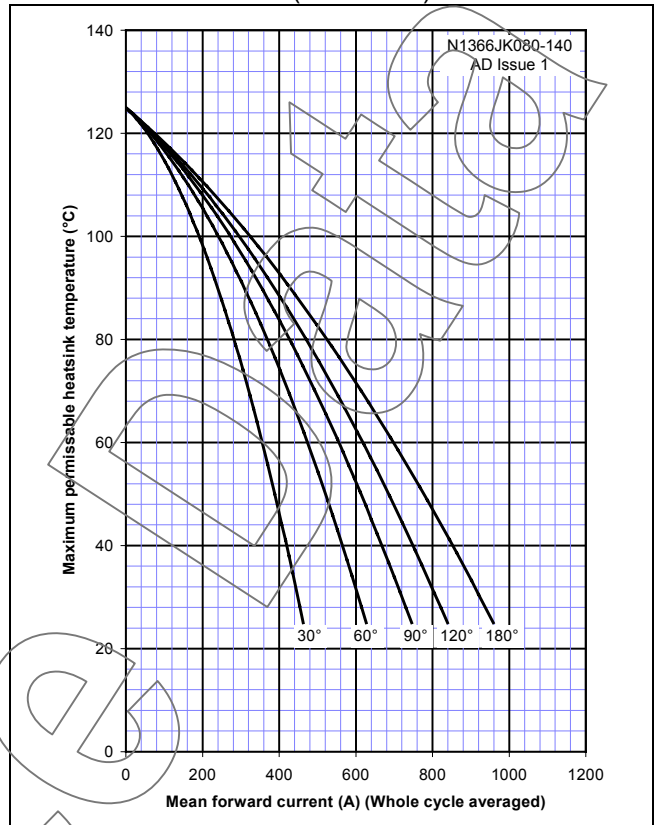


Figure 15 – On-state current vs. Power dissipation – Cathode Side Cooled (Square wave)

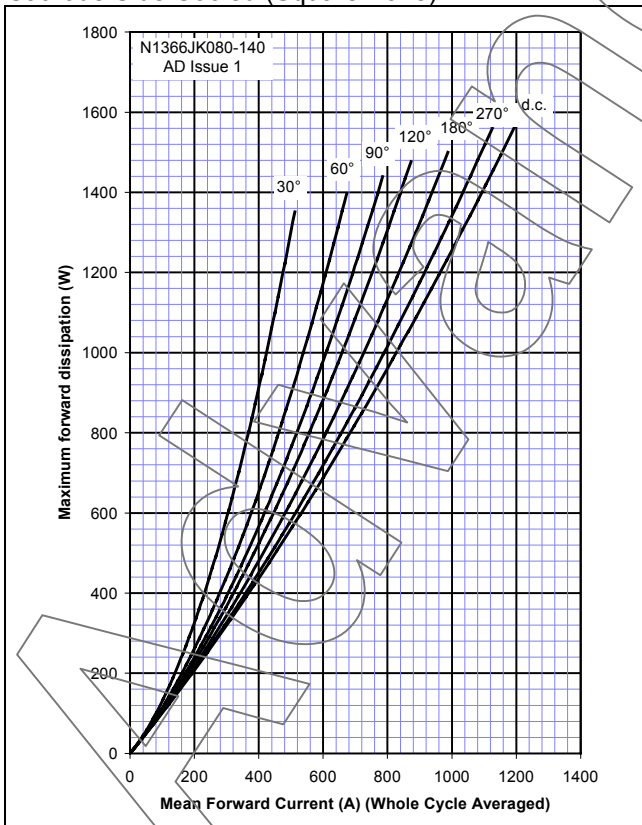


Figure 16 – On-state current vs. Heatsink temperature – Cathode Side Cooled (Square wave)

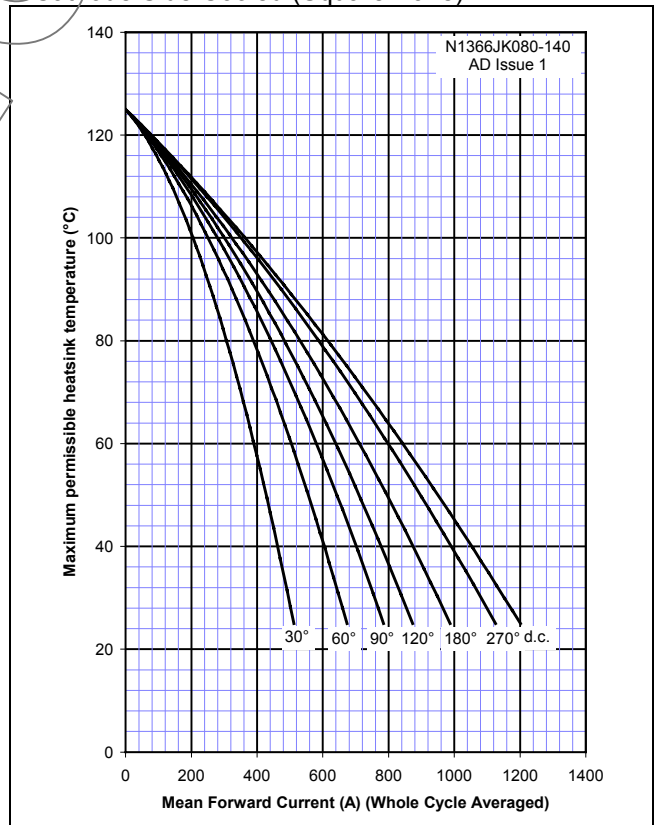
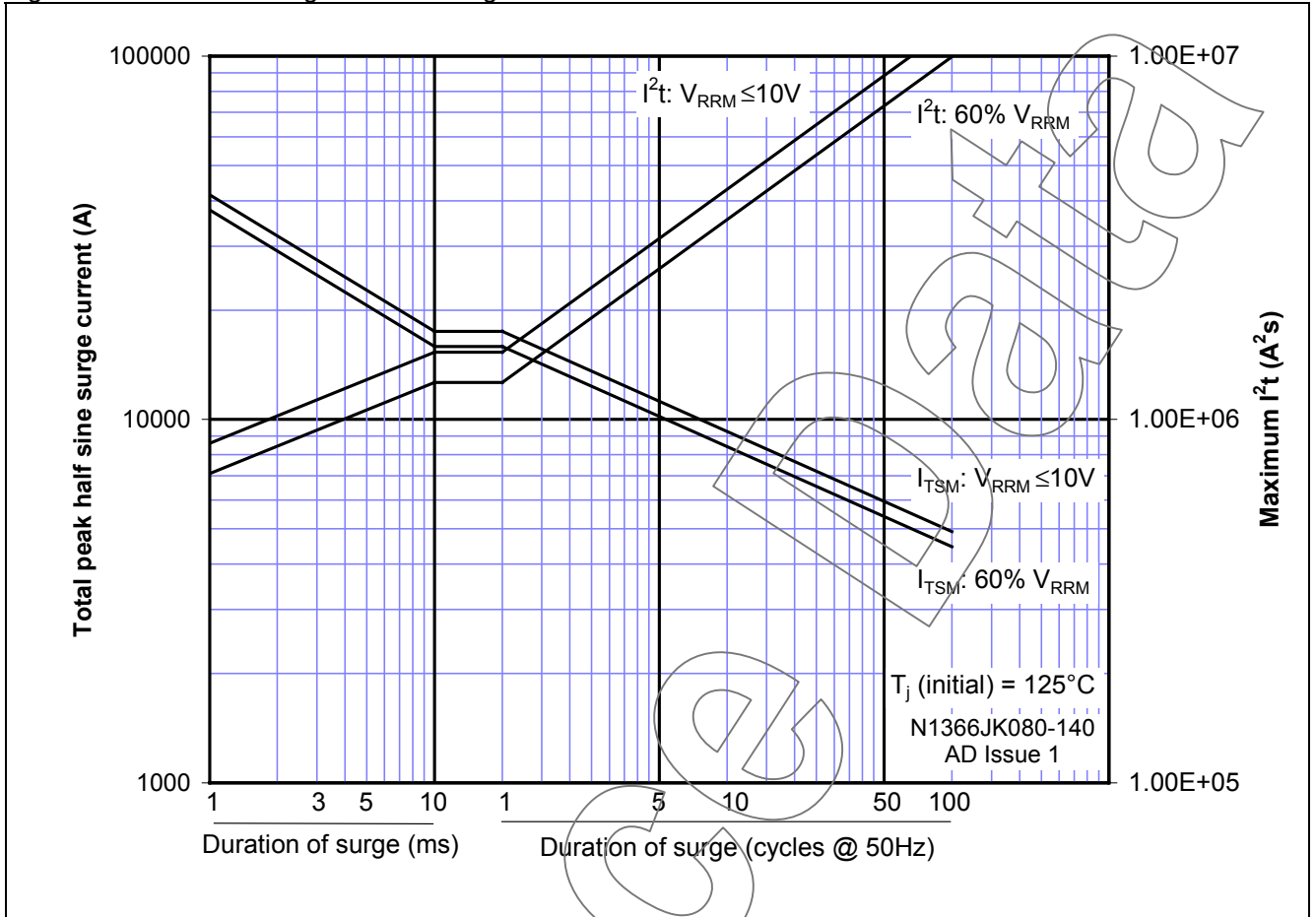
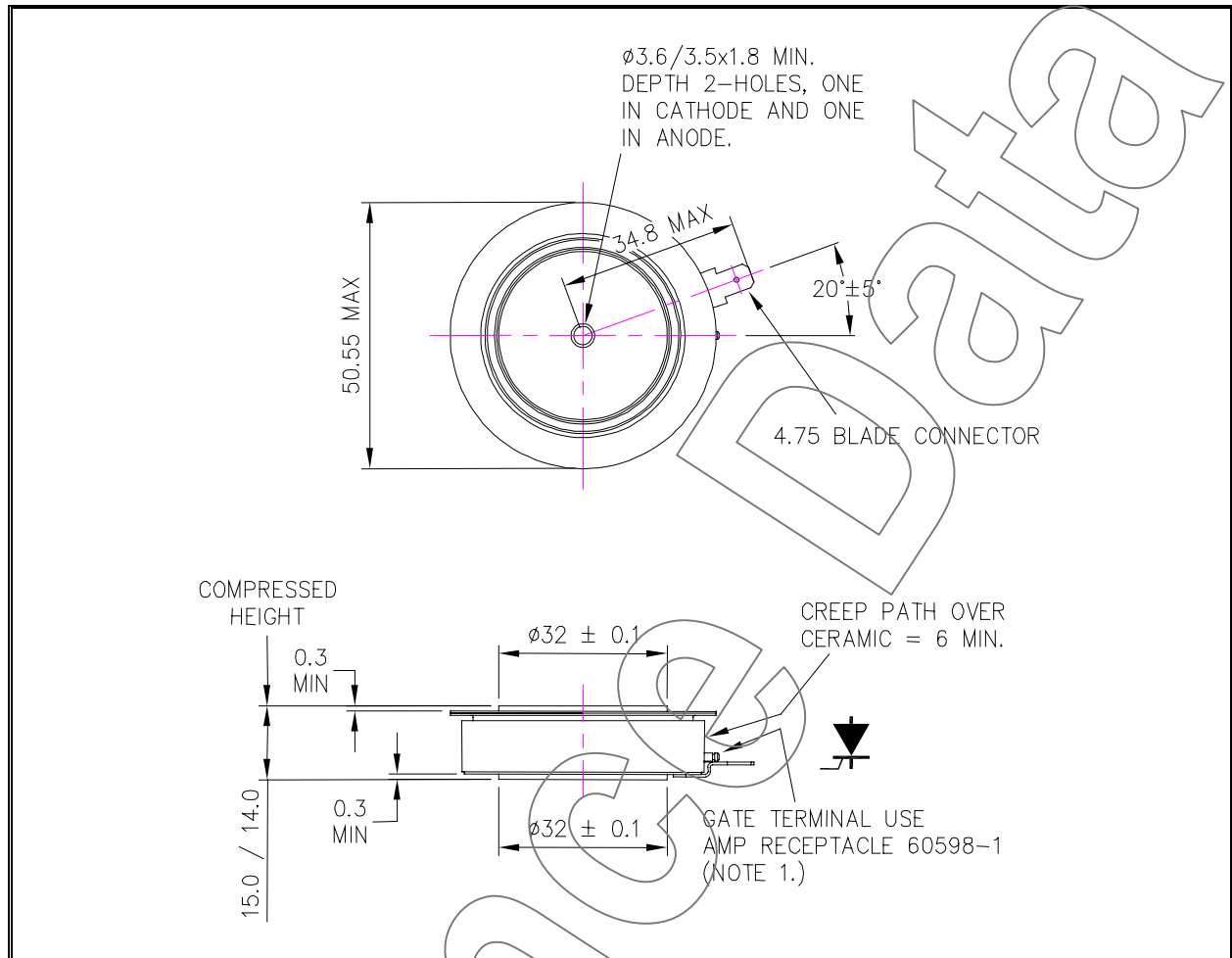


Figure 17 – Maximum surge and  $I^2t$  Ratings



**Outline Drawing & Ordering Information**



ORDERING INFORMATION		(Please quote 10 digit code as below)	
<b>N1366</b>	<b>JK</b>	<b>◆◆</b>	<b>0</b>
Fixed Type Code	Fixed outline code	Voltage code $V_{DRM}/100$ 08-14	Fixed turn-off time code
Order code: N1366JK140 – 1400V $V_{DRM}$ , $V_{RRM}$ , 14mm clamp height capsule.			

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